

AX58101(2) Product Introduction

Revision 1.00
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Revision History

Revision	Date	Description
1.00	2025/08/15	Initial release

Table of Contents

1. Introduction	4
2. Block Diagram	4
3. Target Applications.....	5
4. Order Information	6
5. AX58101(2) Evaluation Board.....	6
5-1. AX58101(2) Evaluation Board	6
6. Hardware/Software Support.....	7

List of Figures

Figure 1. AX58101(2) Block Diagram.....	4
Figure 2. AX58101(2) Target Applications.....	5
Figure 3. Ordering Information	6
Figure 4. AX58101 Evaluation Board	6
Figure 5. AX58101 Evaluation Board Jumpers Setting.....	7

1. Introduction

This document provides an overview of AX58101(2) EtherCAT SubDevice Controller.

The AX58101(2) is an EtherCAT SubDevice Controller (ESC) that integrates two Fast Ethernet PHYs and two MII network interfaces, supporting port 0 and port 2 swapping for flexible network topology. It supports the Local Bus and SPI Slave PDI interfaces to simplify microprocessor connection, and provide a variety of communication and control interfaces including PWM, ABZ/Hall encoder, SPI master, and digital I/O.

The AX58101(2) is interoperable with all EtherCAT systems using standard EtherCAT communication protocols such as CoE, FoE, and VoE. It is suitable for motor/motion control, digital I/O control, sensors data acquisition, robotics, EtherCAT to IO-Link gateways and EtherCAT Junction modules applications.

The AX58101(2) is available in 80-pin LQFP 12x12 mm, 0.8 mm pitch, RoHS compliant package and in operating temperature range from -40 to 105°C.

ASIX offers AX58101(2) evaluation board, demo kit and free Board Support Package (BSP) which includes reference schematics, PCB design guidelines, hardware/software design guides, software tools, sample firmware sources for designers to easily design the AX58101(2) EtherCAT SubDevice products.

2. Block Diagram

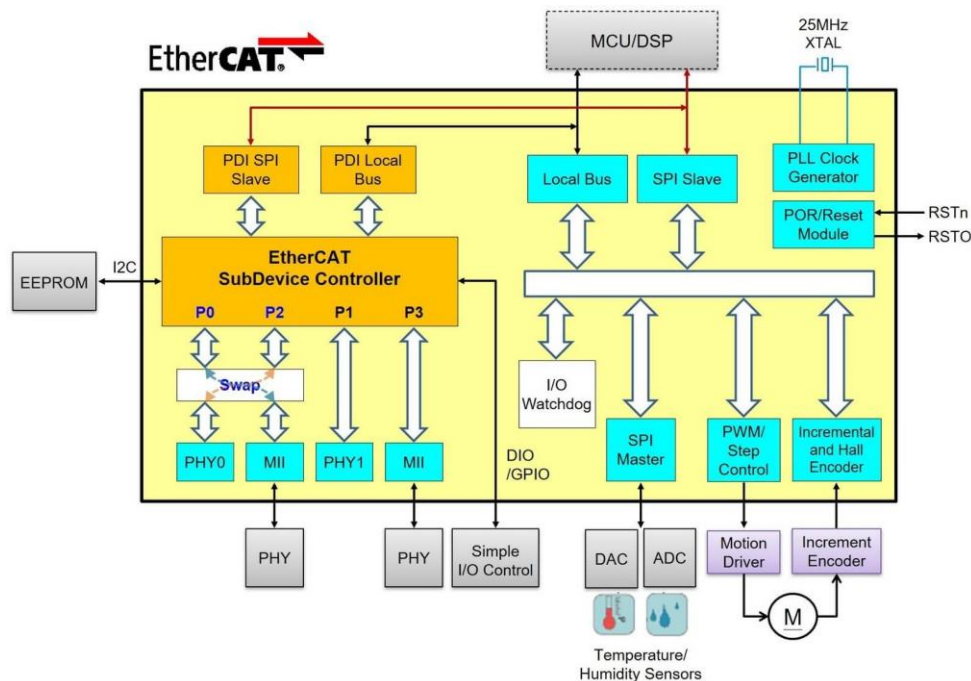


Figure 1. AX58101(2) Block Diagram

3. Target Applications

- Motor/Motion Control
- Digital I/O Control
- Robotics
- Sensors Data Acquisition
- EtherCAT to IO-Link Gateway
- EtherCAT Junction Module
- Communication Module
- Operator HMI Interfaces

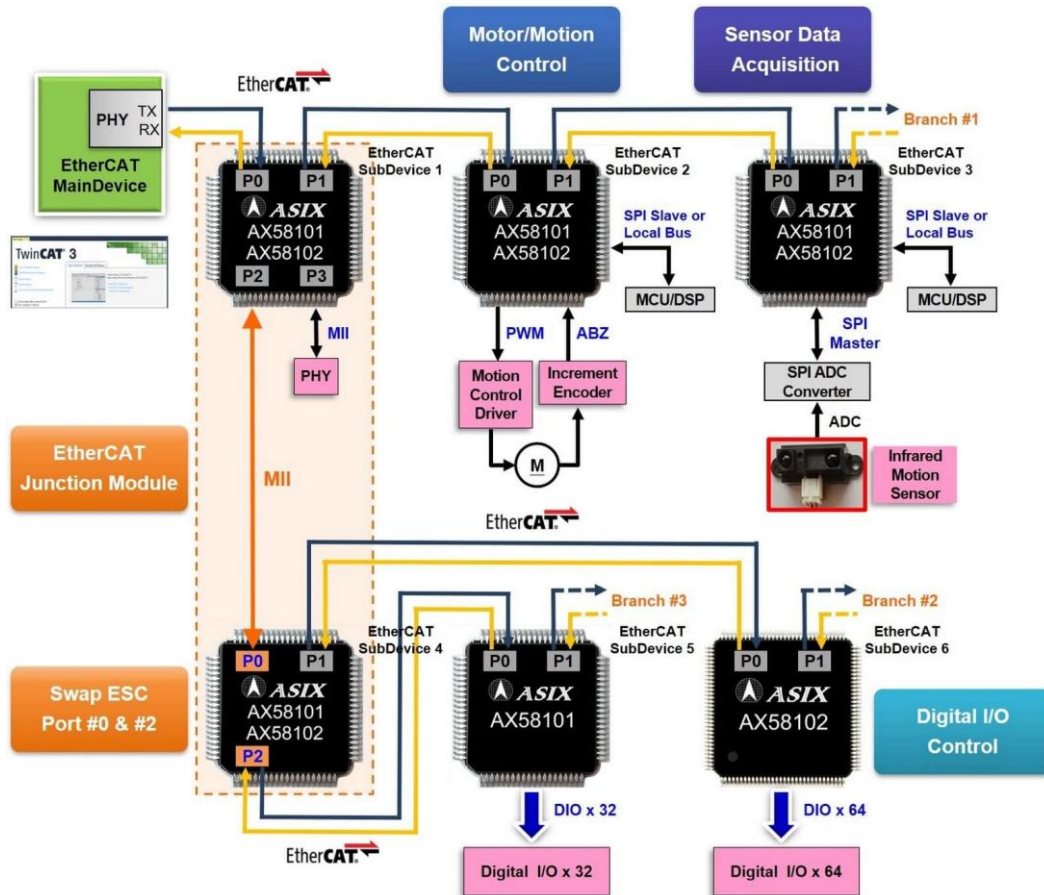


Figure 2. AX58101(2) Target Applications

4. Order Information

The following are the ordering information of AX58101(2) silicon and AX58101(2) evaluation boards. Please contact ASIX's Sales (sales@asix.com.tw) for more details.

Part Number	Description
AX58101 LT	80-pin LQFP lead Free package, Industrial temperature range: -40 to 105°C.

Boards	Description
AX58101-EVB-1	This is AX58101 evaluation board.

Figure 3. Ordering Information

5. AX58101(2) Evaluation Board

ASIX offers AX58101(2) evaluation board for designers to evaluate AX58101(2) functionalities on different target applications.

5-1. AX58101 Evaluation Board

Interface Connector

J1	
GND	1
RSTO	3
GPIO00	5
GPIO02	7
GPIO04	9
GPIO06	11
GPIO08	13
GPIO10	15
GPIO12	17
GPIO14	19
GND	21
GPIO16	23
GPIO18	25
GPIO20	27
GPIO22	29
GPIO24	31
GPIO26	33
GPIO28	35
GPIO30	37
OE EXT	39
OUTVLD	41
EOF	43
SYNC L0	45
LAT IN	47
GND	49
DB 5V	51
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The following is the jumper setting table of the AX58101 Evaluation Board.

Names	Descriptions
P1/P2	EtherCAT SubDevice port 0 & port 1
J3/SW1	DC 5V power jack & switch
SW2	Reset button
J1	Extended interface connector
J2	Pull-up (Short J2.1 & J2.2)/Pull-down (Short J2.2 & J2.3) (default) RSTO signal
J5	Pull-down (Short J5.1 & J5.2)/Pull-up (Short J5.2 & J5.3) (default) I2C EEPROM SCL signal
J6	Pull-down (Short J6.1 & J6.2)/Pull-up (Short J6.2 & J6.3) (default) I2C EEPROM SDA signal

Figure 5. AX58101 Evaluation Board Jumpers Setting

6. Hardware/Software Support

ASIX offers AX58101(2) Board Support Package (BSP) which include reference schematic, PCB layout/gerber/BOM files, application design note and sample TwinCAT PLC demo source/ESI file, etc. Please contact ASIX Sales (sales@asix.com.tw) for details.

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