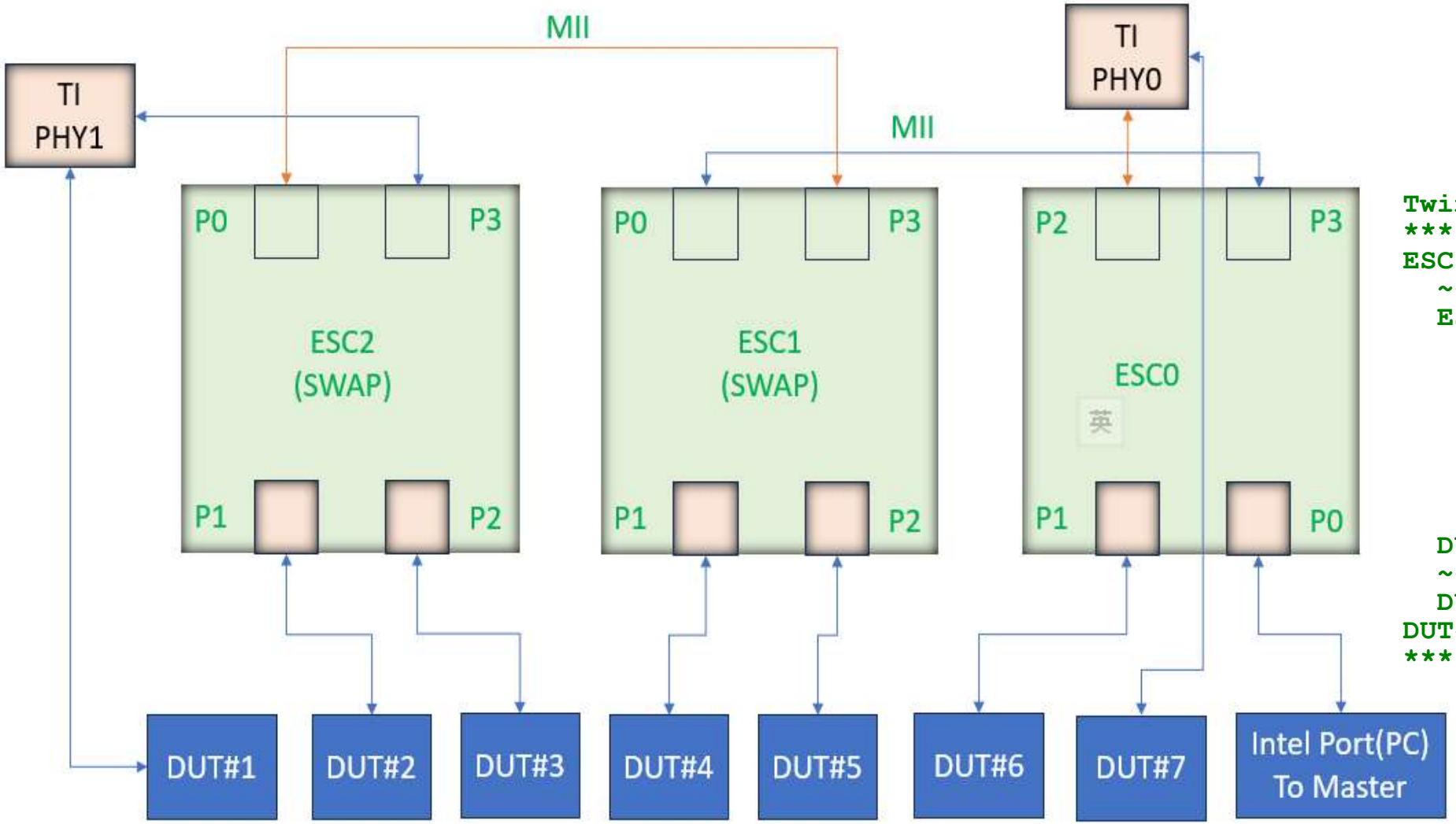
AX58101LT 8Ports Junction Schematic



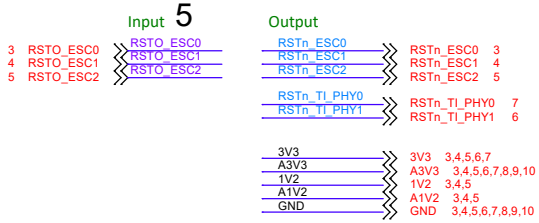

```
TwinCAT:
***********
ESC0
  ~~~~~~~~~~
  ESC1 (SWAP)
    ----------
    ESC2 (SWAP)
      DUT#1
      DUT#2
    DUT#3
    ----------
    DUT#4
  DUT#5
  ~~~~~~~~~~
  DUT#6
DUT#7
***********
```

CN1 CN2 CN3 CN4 CN5 CN6 CN7 CN8

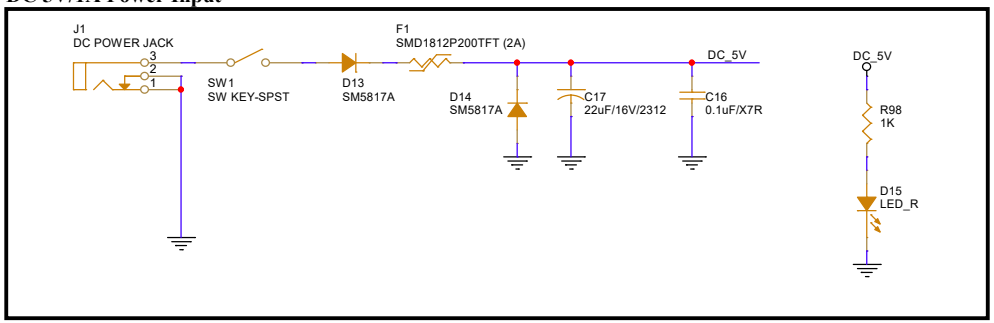
Note:
1.Please deliver us your AX58101 schematic and PCB layout file for further review.

2.Please do full functionalities testing on your own AX58101 board before running into production stage.

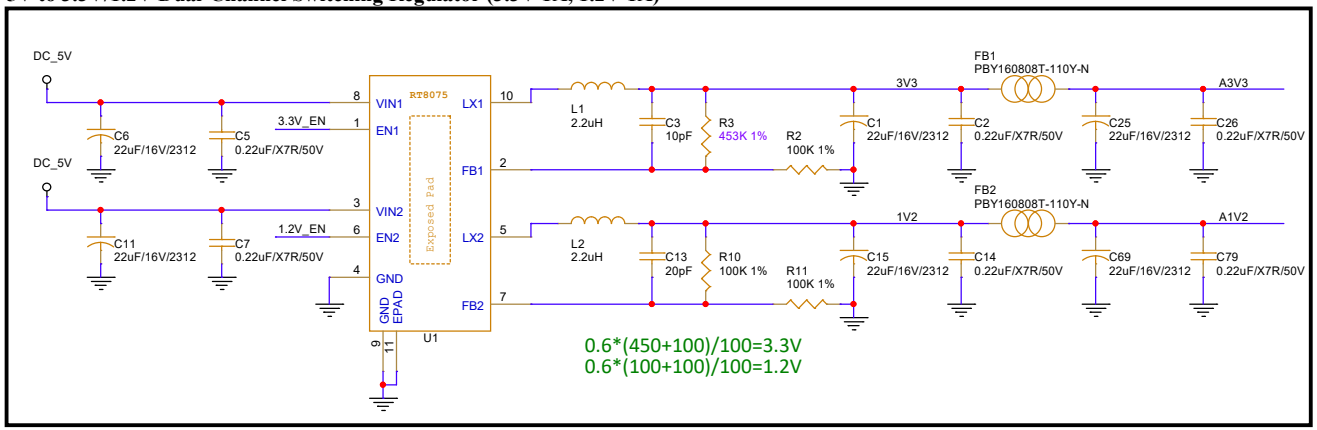
ASIX ELECTRONICS CORPORATION		
Title: P01-System Block		
Size: A3	Document Number: AX58101LT Junction Reference	Rev: 1.00
Date: Monday, August 25, 2025	Sheet 1 of 11	



DC 5V/1A Power Input



5V to 3.3V/1.2V Dual-Channel Switching Regulator (3.3V 1A, 1.2V 1A)



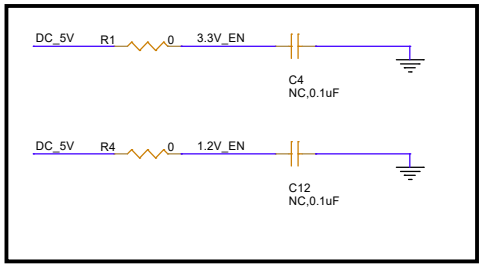
AX58101LT:
1) (A3V3+D3V3)max= 7.53+79.3= 86.83mA.
2) (A1V2+D1V2)max= 64.4+38.7= 103.1mA.
3) 2Copper(P3V3A)max=86mA.

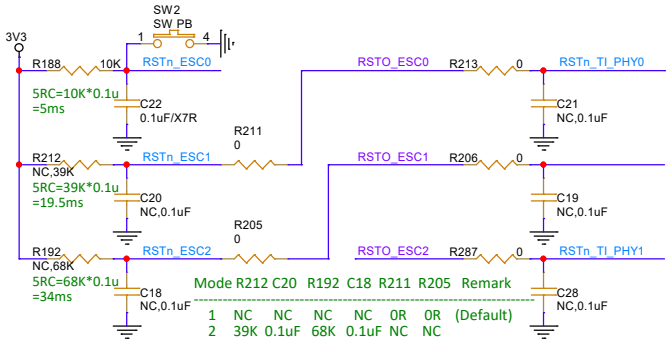
TI PHY(DP83822)(DataSheet)
1) (Magnetic supply)max= 22mA.
2) (AVD supply)max= 52mA.
3) (VDDIO supply)max= 22mA.

3.3V: 1A(Max.)
1) AX58101LT 3pcs: 86.83*3= 260.49mA.
2) 6Copper(P3V3A): 86*6/2= 258mA.
3) TI PHY 2pcs: (22+52+22)*2= 192mA.
4) Total= (260.49+258+192)= 710.49mA.

1.2V: 1A(Max.)
1) AX58101LT 3pcs: 103.1*3= 309.3mA.

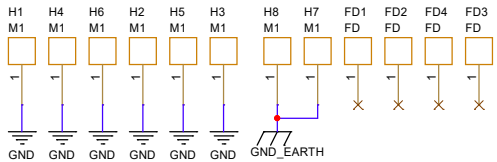
Optional for fining tune power up sequence timing *Note2-1





Mode	R212	C20	R192	C18	R211	R205	Remark
1	NC	NC	NC	NC	0R	0R	(Default)
2	39K	0.1uF	68K	0.1uF	NC	NC	

Mode1:
RSTn_ESC0 超前RSTn_ESC1 10ms.
RSTn_ESC1 超前RSTn_ESC2 9ms.



*Note2-1:
The R1,C4,R4,C12 resistor and capacitors are optional for fining tune the 3V3 and 1V2 power up sequence timing. (Refer to below "3V3 & 1V2 Output Power Timing Setting" table for details.)

ASIX ELECTRONICS CORPORATION		
Title: P02-Power		
Size: A3	Document Number: AX58101LT Junction Reference	Rev: 1.00
Date: Monday, August 25, 2025	Sheet 2 of 11	

P2_TX_EN_ESC0: (4Port Mode)(MSB)
LED_ERR_ESC0: (3Port Mode)(LSB)
2'b00: 2 ports mode
2'b01: 3 ports mode
2'b10: Reserved
2'b11: 4 ports mode

P2_TXD3_ESC0: (SWAP_P0)
MII interface port selection:
0: Select MII2 port to IO. Don't SWAP(P0/P2)
1: Select MII0 port to IO. SWAP(P0/P2)

PDI_EMU_ESC0:
Device emulation
0: Device status register is controlled by PDI.(MCU)
1: Device status register is identical to device control register.(TwinCAT)

RSTO_ESC0: (RSTO_POL)
RSTO Reset Output Polarity:
0: Active Low. (High: Work. Low: Reset)
1: Active High.(Low: Work. High: Reset)

External PHY's TXD phase shift
(TXD[2:1]):
2'b00: Align with MCLK.
2'b01: Delay 1/4 phase with MCLK.
2'b10: Delay 2/4 phase with MCLK.
2'b11: Delay 3/4 phase with MCLK.

P3_TXD0_ESC0: (P3_LINK_POL)
Port3 MII LINK Polarity:
0: Active Low. 1: Active High.

P1_ACT_ESC0: (P1_FIBER)
Port1 PHY Media mode:
0: Copper mode. 1: Fiber mode.

P0_ACT_ESC0: (P0_FIBER)
Port0 PHY Media mode:
0: Copper mode. 1: Fiber mode.

EEP_DONE_ESC0: (FIBER_EN)
PHY 0 and 1 media mode of the PHY mode:
0: Copper mode. 1: Fiber mode.

I2C EEPROM Size (LED_RUN/EEP_SIZE)
0: 1 Kbit to 16Kbit (24C16) => R84,R57,R20,D3 mounted(Default)
1: 32Kbit to 4Mbit (24C32) => R86,R56,R36,D3 mounted

Port3: Connect to ESC1's Port0
Port2: TI PHY

P2_ACT LED

CLKOUT_ESC0:
CLKOUT Enable:
0: Disable. 1: Enable.

P2_TXD0_ESC0:
Port2 MII LINK Polarity:
0: Active Low. (DP83822:CRS Strap Mode=4)
1: Active High. (DP83822:CRS Strap Mode=2)

P2/3_MCLK_ESC0:
MCLK and CLKOUT Driving Select:
0:4mA. 1: 8mA.

*Note3-1:
The R269 resistor of RSET_BG signal MUST be 12K 1%.

*Note3-3:
Please select a proper I2C EEPROM part based on AX58101 pin #79 LED_RUN/EEP_SIZE configuration.

Input

Output

By-pass Capacitors *Note3-4

I2C EEPROM *Note3-3

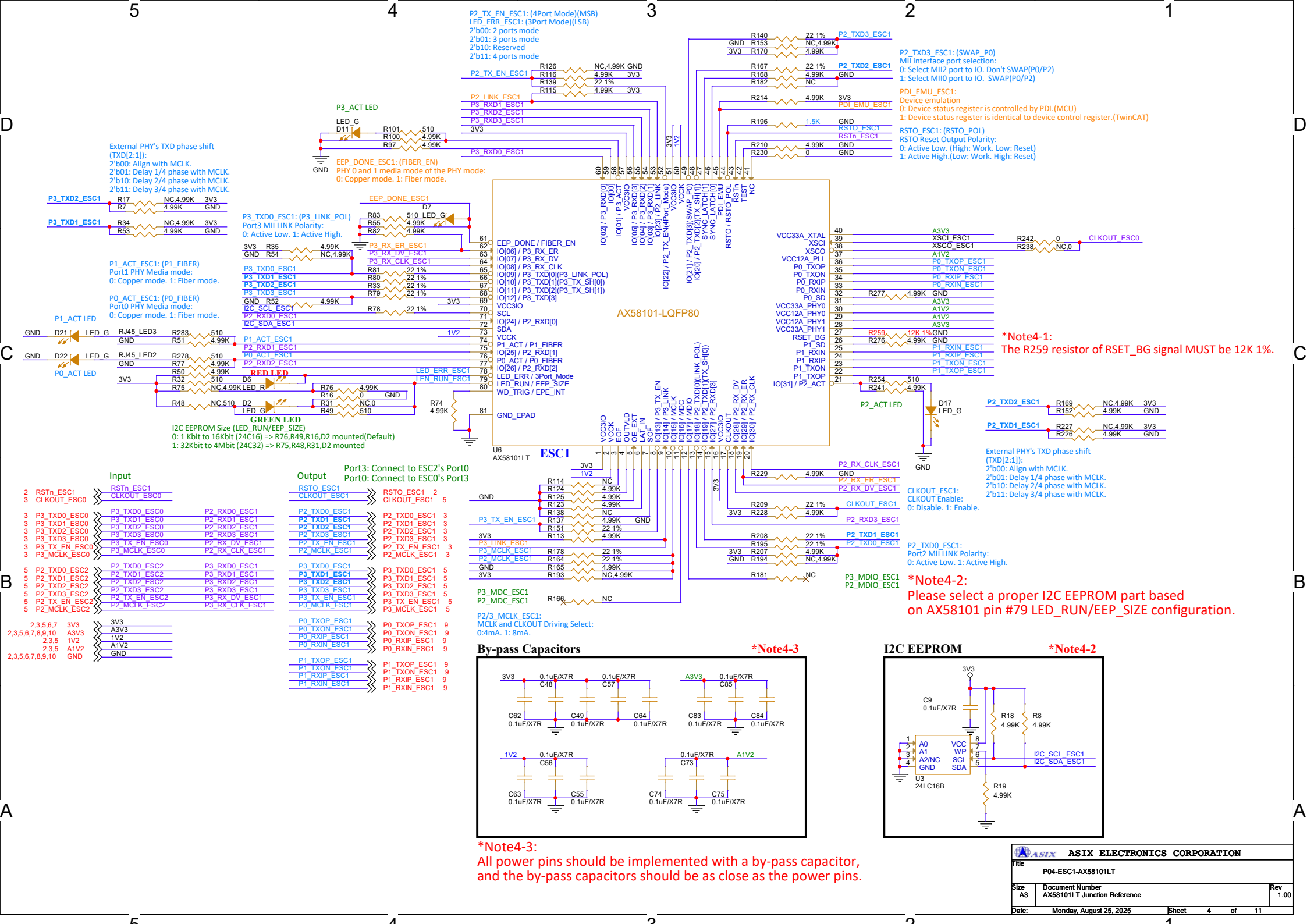
25MHz +/- 30ppm Crystal *Note3-2

*Note3-2:
The reference 25MHz crystal is the NSK NXK25.000AE12F-KAB6-12
SMD 25MHz crystal with CL 12pF, ESR 40 Ohm and Drive Level 100uW.
The 25MHz clock signals should be within 25MHz +- 30ppm.

*Note3-4:
All power pins should be implemented with a by-pass capacitor, and the by-pass capacitors should be as close as the power pins.

Title	P03-ECS0-AX58101LT
Size	A3
Document Number	AX58101LT Junction Reference
Rev	1.00
Date:	Monday, August 25, 2025
Sheet	3 of 11

ASIX ELECTRONICS CORPORATION


P2_TX_EN_ESC1: (4Port Mode)(MSB)
LED_ERR_ESC1: (3Port Mode)(LSB)
2'b00: 2 ports mode
2'b01: 3 ports mode
2'b10: Reserved
2'b11: 4 ports mode
P2_TXD3_ESC1: (SWAP_P0)
MII interface port selection:
0: Select MII2 port to IO. Don't SWAP(P0/P2)
1: Select MII0 port to IO. SWAP(P0/P2)
PDI_EMU_ESC1:
Device emulation
0: Device status register is controlled by PDI.(MCU)
1: Device status register is identical to device control register.(TwinCAT)
RSTO_ESC1: (RSTO_POL)
RSTO Reset Output Polarity:
0: Active Low. (High: Work. Low: Reset)
1: Active High.(Low: Work. High: Reset)
P3_ACT LED
EEP_DONE_ESC1: (FIBER_EN)
PHY 0 and 1 media mode of the PHY mode:
0: Copper mode. 1: Fiber mode.
External PHY's TXD phase shift
(TXD[2:1]):
2'b00: Align with MCLK.
2'b01: Delay 1/4 phase with MCLK.
2'b10: Delay 2/4 phase with MCLK.
2'b11: Delay 3/4 phase with MCLK.
P3_TXD0_ESC1: (P3_LINK_POL)
Port3 MII LINK Polarity:
0: Active Low. 1: Active High.
P1_ACT_ESC1: (P1_FIBER)
Port1 PHY Media mode:
0: Copper mode. 1: Fiber mode.
P0_ACT_ESC1: (P0_FIBER)
Port0 PHY Media mode:
0: Copper mode. 1: Fiber mode.
P1_ACT LED
P0_ACT LED
RED LED
GREEN LED
I2C EEPROM Size (LED_RUN/EEP_SIZE)
0: 1 Kbit to 16Kbit (24C16) => R76,R49,R16,D2 mounted(Default)
1: 32Kbit to 4Mbit (24C32) => R75,R48,R31,D2 mounted
AX58101-LQFP80
U6
AX58101LT
ESC1
P2_ACT LED
D17
LED_G
*Note4-1:
The R259 resistor of RSET_BG signal MUST be 12K 1%.
CLKOUT_ESC1:
CLKOUT Enable:
0: Disable. 1: Enable.
P2_TXD0_ESC1:
Port2 MII LINK Polarity:
0: Active Low. 1: Active High.
*Note4-2:
Please select a proper I2C EEPROM part based
on AX58101 pin #79 LED_RUN/EEP_SIZE configuration.
P2/3_MCLK_ESC1:
MCLK and CLKOUT Driving Select:
0:4mA. 1: 8mA.
Input
Output
Port3: Connect to ESC2's Port0
Port0: Connect to ESC0's Port3
By-pass Capacitors
*Note4-3
I2C EEPROM
*Note4-2
U3
24LC16B
*Note4-3:
All power pins should be implemented with a by-pass capacitor,
and the by-pass capacitors should be as close as the power pins.
ASIX ELECTRONICS CORPORATION
Title
P04-ESC1-AX58101LT
Size
A3
Document Number
AX58101LT Junction Reference
Rev
1.00
Date:
Monday, August 25, 2025
Sheet
4
of
11

P2_TX_EN_ESC2: (4Port Mode)(MSB)
LED_ERR_ESC2: (3Port Mode)(LSB)
2'b00: 2 ports mode
2'b01: 3 ports mode
2'b10: Reserved
2'b11: 4 ports mode

P2_TXD3_ESC2: (SWAP_P0)
MII interface port selection:
0: Select MII2 port to IO. Don't SWAP(P0/P2)
1: Select MII0 port to IO. SWAP(P0/P2)

PDI_EMU_ESC2:
Device emulation
0: Device status register is controlled by PDI.(MCU)
1: Device status register is identical to device control register.(TwinCAT)

RSTO_ESC2: (RSTO_POL)
RSTO Reset Output Polarity:
0: Active Low. (High: Work. Low: Reset)
1: Active High.(Low: Work. High: Reset)

External PHY's TXD phase shift
(TXD[2:1]):
2'b00: Align with MCLK.
2'b01: Delay 1/4 phase with MCLK.
2'b10: Delay 2/4 phase with MCLK.
2'b11: Delay 3/4 phase with MCLK.

P3_ACT LED

EEP_DONE_ESC2: (FIBER_EN)
PHY 0 and 1 media mode of the PHY mode:
0: Copper mode. 1: Fiber mode.

P3_TXD0_ESC2: (P3_LINK_POL)
Port3 MII LINK Polarity:
0: Active Low. 1: Active High.

P1_ACT_ESC2: (P1_FIBER)
Port1 PHY Media mode:
0: Copper mode. 1: Fiber mode.

P0_ACT_ESC2: (P0_FIBER)
Port0 PHY Media mode:
0: Copper mode. 1: Fiber mode.

P1_ACT LED

P0_ACT LED

RED LED

GREEN LED

I2C EEPROM Size (LED_RUN/EEP_SIZE)
0: 1 Kbit to 16Kbit (24C16) => R66,R41,R12,D1 mounted(Default)
1: 32Kbit to 4Mbit (24C32) => R64,R40,R26,D1 mounted

Port3: TI PHY
Port0: Connect to ESC1's Port3

AX58101-LQFP80

U5
AX58101LT
ESC2

P2_ACT LED

*Note5-1:
The R249 resistor of RSET_BG signal MUST be 12K 1%.

*Note5-2:
Please select a proper I2C EEPROM part based on AX58101 pin #79 LED_RUN/EEP_SIZE configuration.

CLKOUT_ESC2:
CLKOUT Enable:
0: Disable. 1: Enable.

P2_TXD0_ESC2:
Port2 MII LINK Polarity:
0: Active Low. 1: Active High.

P2/3_MCLK_ESC2:
MCLK and CLKOUT Driving Select:
0:4mA. 1: 8mA.

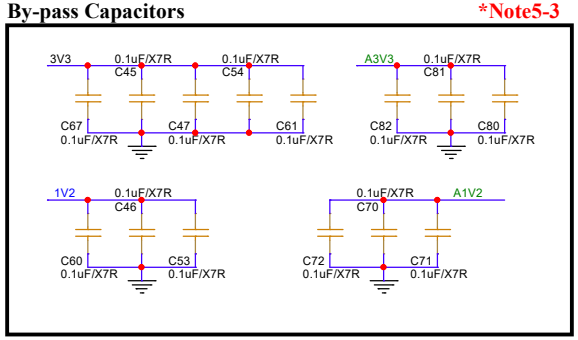
Input

2	RSTn_ESC2	RSTn_ESC2	
4	CLKOUT_ESC1	CLKOUT_ESC1	
4	P3_TXD0_ESC1	P3_TXD0_ESC1	P2_RXD0_ESC2
4	P3_TXD1_ESC1	P3_TXD1_ESC1	P2_RXD1_ESC2
4	P3_TXD2_ESC1	P3_TXD2_ESC1	P2_RXD2_ESC2
4	P3_TXD3_ESC1	P3_TXD3_ESC1	P2_RXD3_ESC2
4	P3_TX_EN_ESC1	P3_TX_EN_ESC1	P2_RX_DV_ESC2
4	P3_MCLK_ESC1	P3_MCLK_ESC1	P2_RX_CLK_ESC2
6	RXD0_ESC2	RXD0_ESC2	P3_RXD0_ESC2
6	RXD1_ESC2	RXD1_ESC2	P3_RXD1_ESC2
6	RXD2_ESC2	RXD2_ESC2	P3_RXD2_ESC2
6	RXD3_ESC2	RXD3_ESC2	P3_RXD3_ESC2
6	RX_DV_ESC2	RX_DV_ESC2	P3_RX_DV_ESC2
6	RX_CLK_ESC2	RX_CLK_ESC2	P3_RX_CLK_ESC2
6	RX_ER_ESC2	RX_ER_ESC2	P3_RX_ER_ESC2
6	LINK_ESC2	LINK_ESC2	P3_LINK_ESC2
2,3,4,6,7	3V3	3V3	
2,3,4,6,7,8,9,10	A3V3	A3V3	
2,3,4	1V2	1V2	
2,3,4	A1V2	A1V2	
2,3,4,6,7,8,9,10	GND	GND	

Output

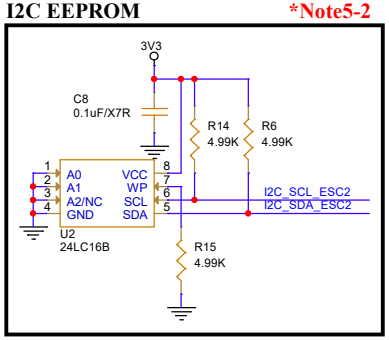
RSTO_ESC2	RSTO_ESC2	2
P2_TXD0_ESC2	P2_TXD0_ESC2	4
P2_TXD1_ESC2	P2_TXD1_ESC2	4
P2_TXD2_ESC2	P2_TXD2_ESC2	4
P2_TXD3_ESC2	P2_TXD3_ESC2	4
P2_TX_EN_ESC2	P2_TX_EN_ESC2	4
P2_MCLK_ESC2	P2_MCLK_ESC2	4
P3_TXD0_ESC2	P3_TXD0_ESC2	6
P3_TXD1_ESC2	P3_TXD1_ESC2	6
P3_TXD2_ESC2	P3_TXD2_ESC2	6
P3_TXD3_ESC2	P3_TXD3_ESC2	6
P3_TX_EN_ESC2	P3_TX_EN_ESC2	6
P3_MCLK_ESC2	P3_MCLK_ESC2	6
P3_MDIO_ESC2	P3_MDIO_ESC2	6
P3_MDC_ESC2	P3_MDC_ESC2	6
P0_TXOP_ESC2	P0_TXOP_ESC2	10
P0_TXON_ESC2	P0_TXON_ESC2	10
P0_RXIP_ESC2	P0_RXIP_ESC2	10
P0_RXIN_ESC2	P0_RXIN_ESC2	10
P1_TXOP_ESC2	P1_TXOP_ESC2	10
P1_TXON_ESC2	P1_TXON_ESC2	10
P1_RXIP_ESC2	P1_RXIP_ESC2	10
P1_RXIN_ESC2	P1_RXIN_ESC2	10

By-pass Capacitors *Note5-3



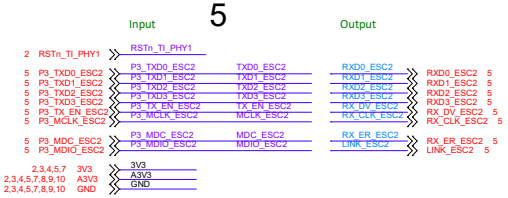
*Note5-3:
All power pins should be implemented with a by-pass capacitor, and the by-pass capacitors should be as close as the power pins.

I2C EEPROM *Note5-2



Title	P05-ESC2-AX58101LT
Size	A3
Document Number	AX58101LT Junction Reference
Rev	1.00
Date:	Monday, August 25, 2025
Sheet	5 of 11

ASIX ELECTRONICS CORPORATION

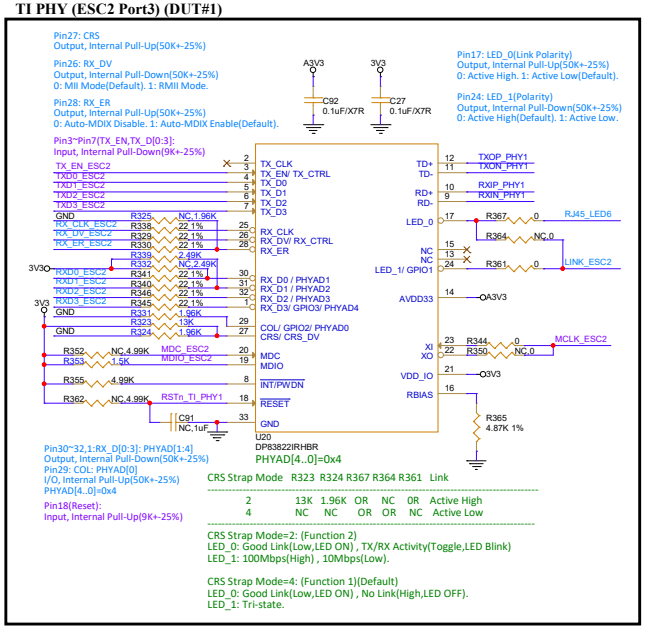


8-11 Modes of Operation				
FX_EN	AN_EN	AN_1	AN_0	Description
Force Modes				
0	0	0	0	10BASE-Te, Half-Duplex
0	0	0	1	10BASE-Te, Full-Duplex
0	0	1	0	100BASE-TX, Half-Duplex
0	0	1	1	100BASE-TX, Full-Duplex
Advertised Modes				
0	1	0	0	10BASE-Te, Half-Duplex
0	1	0	1	10BASE-Te, Half/Full-Duplex
0	1	1	0	10BASE-Te, Half-Duplex 100BASE-TX, Half-Duplex
0	1	1	1	10BASE-Te, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex
Fiber Modes				
1	X	X	0	100BASE-FX, Half Duplex
1	X	X	1	100BASE-FX, Full Duplex

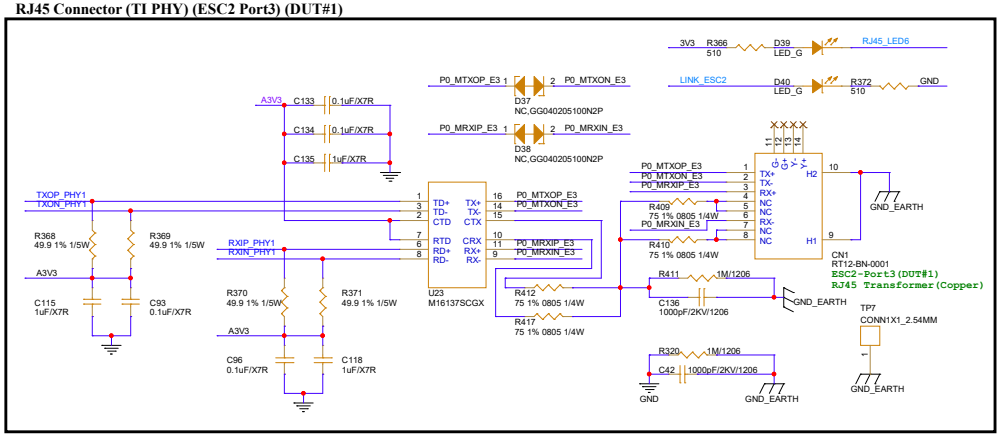
8-12 LED Configuration				
CRS Strap Mode	LED_SPEED	LED_CFG[0]	LED_0	LED_1
1	0	0	ON for Good Link BLINK for TX/RX Activity	LED_1 in Tri-State
2	1	0	ON for Good Link BLINK for TX/RX Activity	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED
3	1	1	ON for Good Link OFF for No Link	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED
4	0	1	ON for Good Link OFF for No Link	LED_1 in Tri-State

8-13 MAC Interface Configuration			
RGMII_EN	RMII_EN	XI_50	Description
0	0	0	MII, 25-MHz Reference Clock
0	0	1	Reserved
0	1	0	RMII, 25-MHz Reference Clock
0	1	1	RMII, 50-MHz Reference Clock
1	X	0	RGMII, 25-MHz Reference Clock
1	X	1	Reserved

TI PHY (ESC2 Port3) (DUT#1)

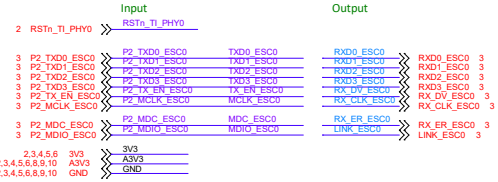


RJ45 Connector (TI PHY) (ESC2 Port3) (DUT#1)

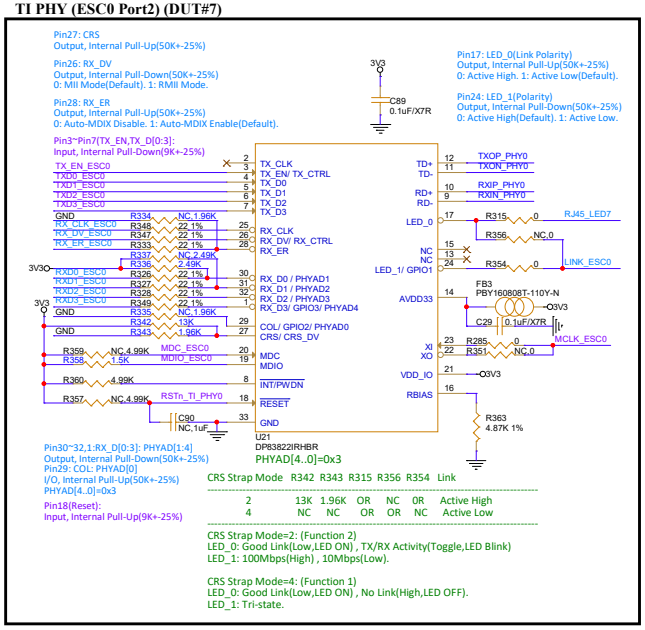


PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			PU Resistor (kΩ)	PD Resistor (kΩ)	TI PHY0 Address 0x3	TI PHY1 Address 0x4	Internal Pull
COL	29	[01]	MODE	FX_EN	PHY_AD0					Up 50K
			1	0	0	OPEN	1.96		v	
			2	1	0	13	1.96			
			3	1	1	6.2	1.96			
			4(Default)	0	1	OPEN	OPEN	v		
CRS	27	[01]	MODE	LED_SPEED	LED_CFG					Up 50K
			1	0	0	OPEN	1.96			
			2	1	0	13	1.96	v	v	
			3	1	1	6.2	1.96			
			4(Default)	0	1	OPEN	OPEN			
RX_ER	28	[01]	MODE	RGMII_EN	AMDIX_EN (SD_EN)					Up 50K
			1	0	0	OPEN	1.96			
			2	1	0	13	1.96			
			3	1	1	6.2	1.96			
			4(Default)	0	1	OPEN	OPEN	v	v	
LED_0	17	[X1]	MODE	RESERVED	AN_0					Up 50K
			1	X	0	OPEN	1.96			
			2	X	Do Not Use(1)	13	1.96			
			3	X	Do Not Use(1)	6.2	1.96			
			4(Default)	X	1	OPEN	OPEN	v	v	
RX_D0	30	[10]	MODE	AN_1	PHY_AD1					Down 50K
			1(Default)	1	0	OPEN	OPEN		v	
			2	0	0	10	2.49			
			3	0	1	5.76	2.49			
			4	1	1	2.49	OPEN	v		
RX_D1	31	[00]	MODE	EEE_EN	PHY_AD2					Down 50K
			1(Default)	0	0	OPEN	OPEN	v		
			2	1	0	10	2.49			
			3	1	1	5.76	2.49			
			4	0	1	2.49	OPEN		v	
RX_D2	32	[00]	MODE	FLD_EN	PHY_AD3					Down 50K
			1(Default)	0	0	OPEN	OPEN	v	v	
			2	1	0	10	2.49			
			3	1	1	5.76	2.49			
			4	0	1	2.49	OPEN			
RX_D3	1	[10]	MODE	AN_EN	PHY_AD4					Down 50K
			1(Default)	1	0	OPEN	OPEN	v	v	
			2	0	0	10	2.49			
			3	0	1	5.76	2.49			
			4	1	1	2.49	OPEN			
RX_DV	26	[00]	MODE	XI_50	RMII_EN					Down 50K
			1(Default)	0	0	OPEN	OPEN	v	v	
			2	1	0	10	2.49			
			3	0	1	5.76	2.49			
			4	1	1	2.49	OPEN			
LED_1	24	[1X]	MODE	RESERVED						Down 50K
			1(Default)	0		OPEN	OPEN	v	v	
			2	Do Not Use(1)		10	2.49			
			3	Do Not Use(1)		5.76	2.49			
			4	1		2.49	OPEN			

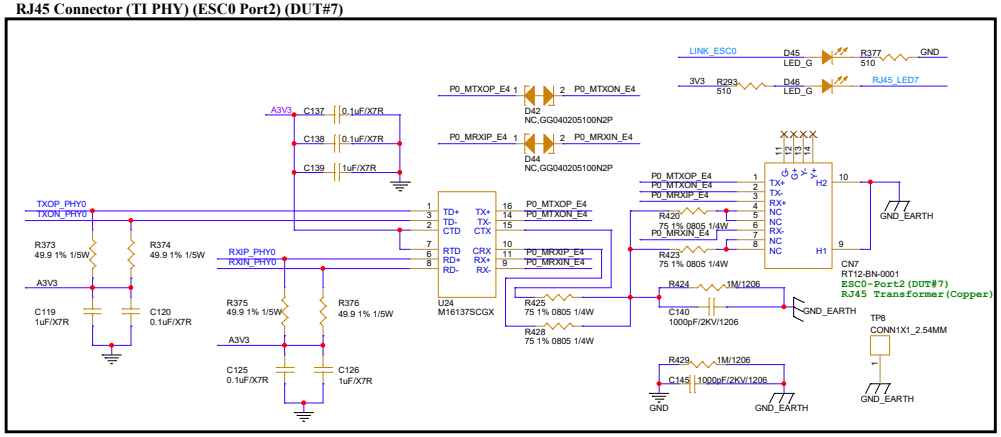
ASIX ELECTRONICS CORPORATION			
Title: P06-TI PHY-DUT1			
Size: A2	Document Number: AXS8101LT Junction Reference		Rev: 1.00
Date: Monday, August 25, 2025	Sheet 6 of 11		



TI PHY (ESC0 Port2) (DUT#7)



RJ45 Connector (TI PHY) (ESC0 Port2) (DUT#7)



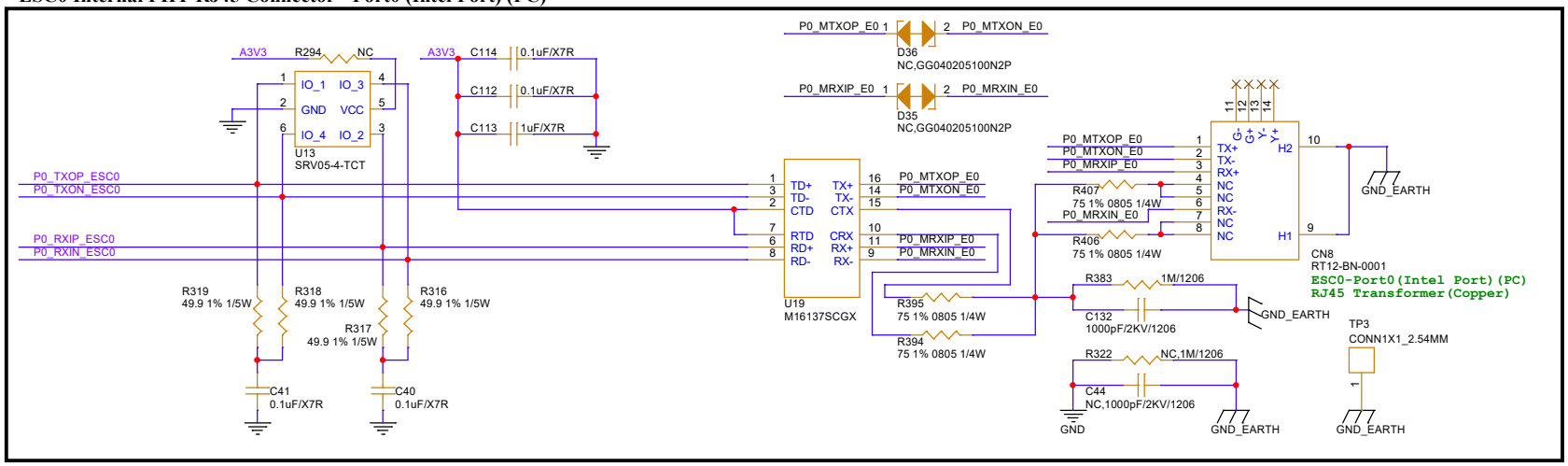
ASIX ELECTRONICS CORPORATION		
Title: P07-TI PHY-DUT7		
Size: A2	Document Number: AX58101LT Junction Reference	Rev: 1.00
Date: Monday, August 25, 2025	Sheet 7 of 11	

3 P0_TXOP_ESC0 — P0_TXOP_ESC0
3 P0_TXON_ESC0 — P0_TXON_ESC0
3 P0_RXIP_ESC0 — P0_RXIP_ESC0
3 P0_RXIN_ESC0 — P0_RXIN_ESC0

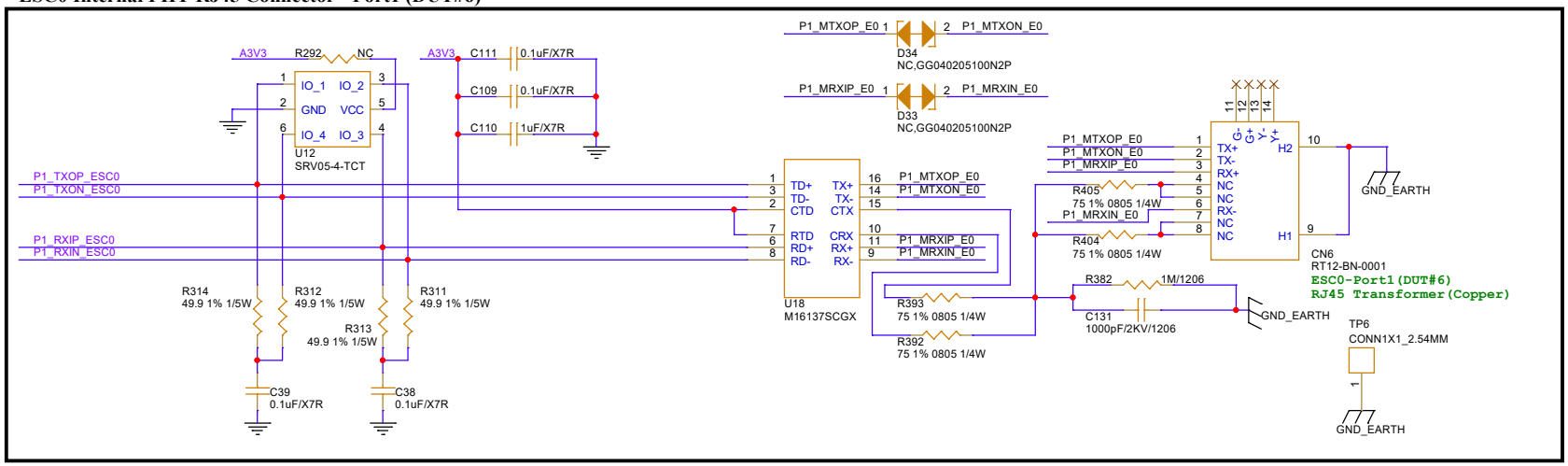
3 P1_TXOP_ESC0 — P1_TXOP_ESC0
3 P1_TXON_ESC0 — P1_TXON_ESC0
3 P1_RXIP_ESC0 — P1_RXIP_ESC0
3 P1_RXIN_ESC0 — P1_RXIN_ESC0

2,3,4,5,6,7,9,10 A3V3 — A3V3
2,3,4,5,6,7,9,10 GND — GND

ESC0 Internal PHY RJ45 Connector - Port0 (Intel Port) (PC)



ESC0 Internal PHY RJ45 Connector - Port1 (DUT#6)



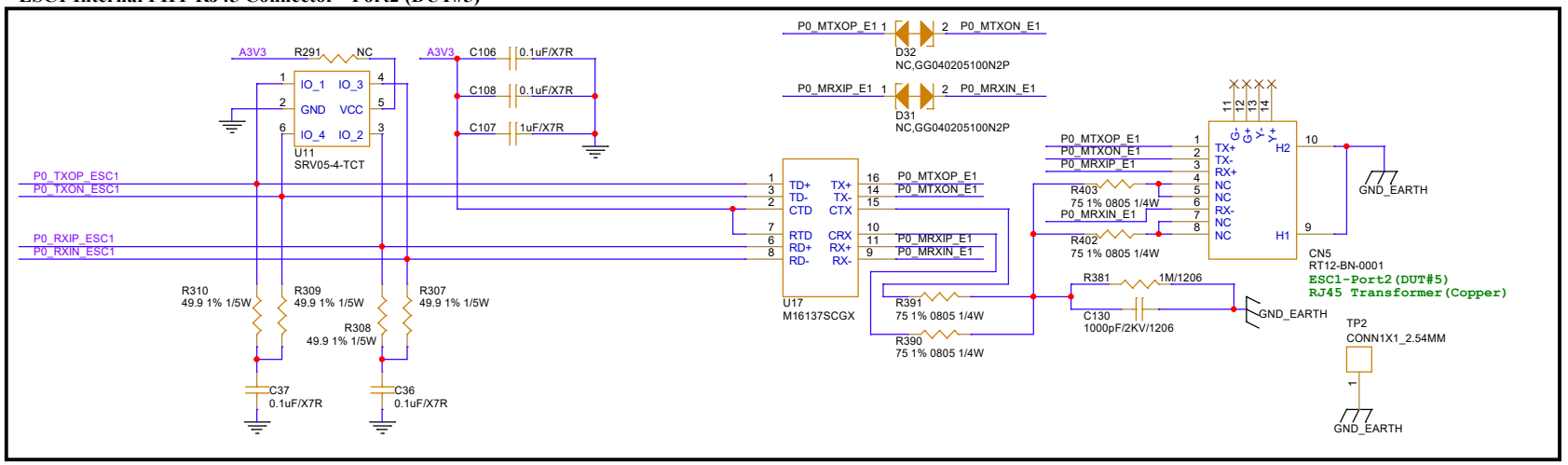
ASIX ELECTRONICS CORPORATION		
Title: P08-INT. PHY-DUT6-PC		
Size: A3	Document Number: AX58101LT Junction Reference	Rev: 1.00
Date: Tuesday, August 26, 2025	Sheet 8 of 11	

4 P0_TXOP_ESC1 — P0_TXOP_ESC1
4 P0_TXON_ESC1 — P0_TXON_ESC1
4 P0_RXIP_ESC1 — P0_RXIP_ESC1
4 P0_RXIN_ESC1 — P0_RXIN_ESC1

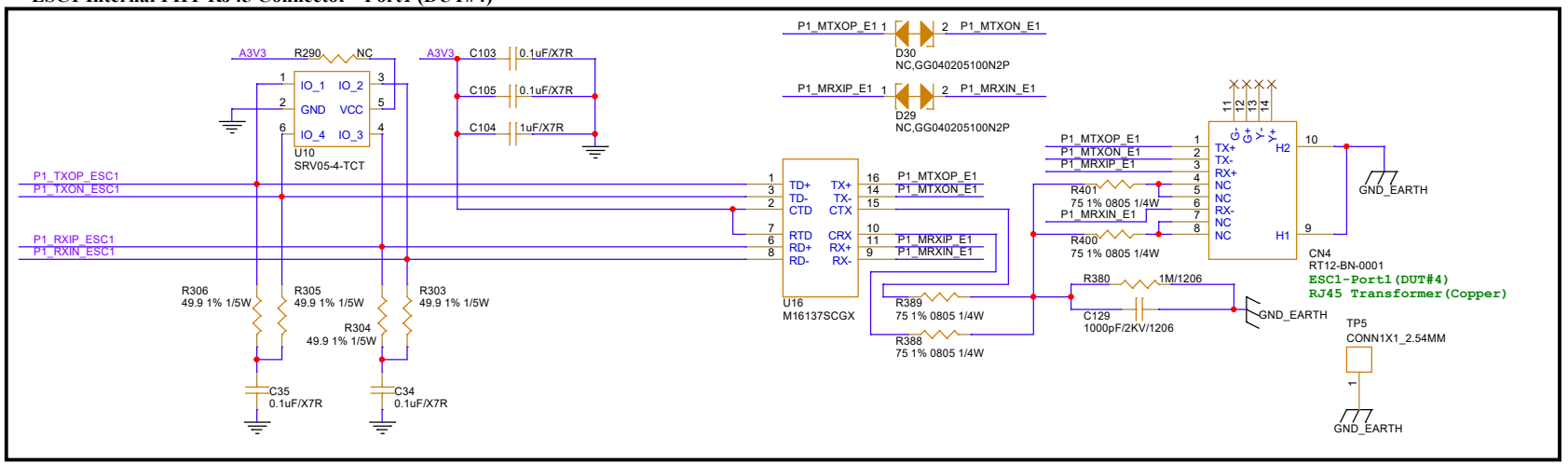
4 P1_TXOP_ESC1 — P1_TXOP_ESC1
4 P1_TXON_ESC1 — P1_TXON_ESC1
4 P1_RXIP_ESC1 — P1_RXIP_ESC1
4 P1_RXIN_ESC1 — P1_RXIN_ESC1

2,3,4,5,6,7,8,10 A3V3 — A3V3
2,3,4,5,6,7,8,10 GND — GND

ESC1 Internal PHY RJ45 Connector - Port2 (DUT#5)



ESC1 Internal PHY RJ45 Connector - Port1 (DUT#4)



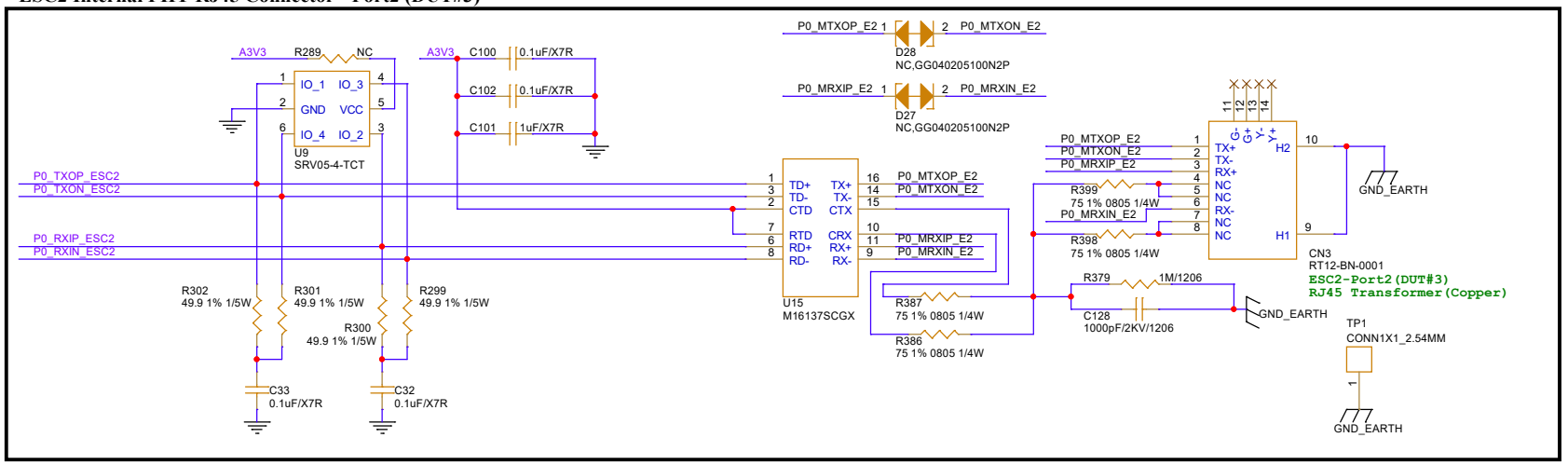
ASIX ELECTRONICS CORPORATION		
Title: P09-INT. PHY-DUT4/5		
Size: A3	Document Number: AX58101LT Junction Reference	Rev: 1.00
Date: Monday, August 25, 2025	Sheet 9 of 11	

5 P0_TXOP_ESC2 — P0_TXOP_ESC2
5 P0_TXON_ESC2 — P0_TXON_ESC2
5 P0_RXIP_ESC2 — P0_RXIP_ESC2
5 P0_RXIN_ESC2 — P0_RXIN_ESC2

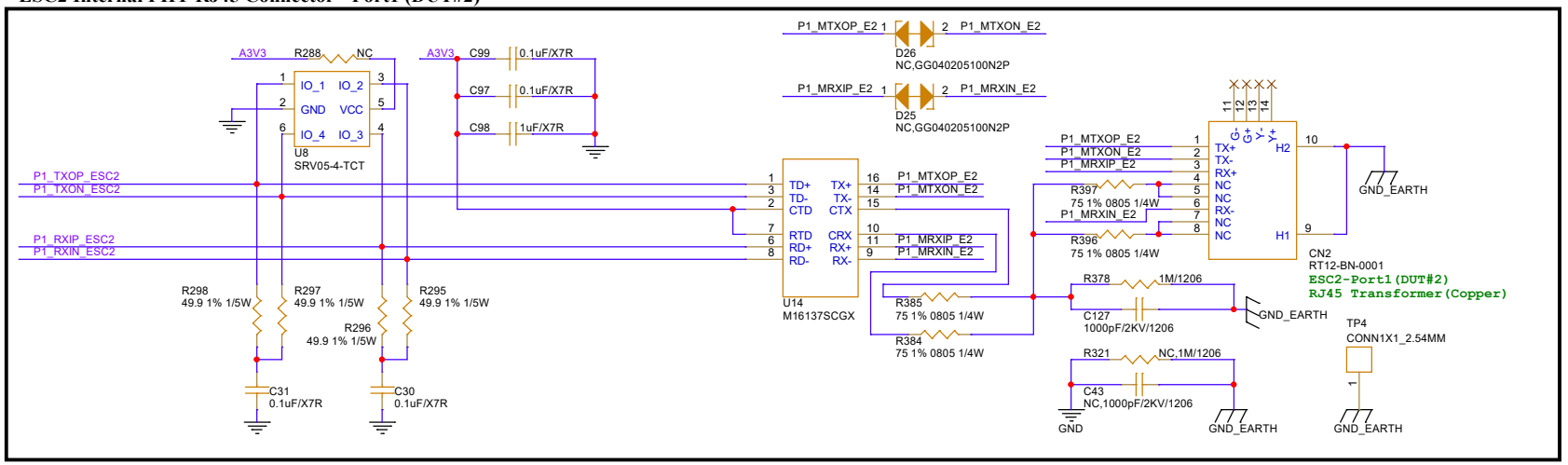
5 P1_TXOP_ESC2 — P1_TXOP_ESC2
5 P1_TXON_ESC2 — P1_TXON_ESC2
5 P1_RXIP_ESC2 — P1_RXIP_ESC2
5 P1_RXIN_ESC2 — P1_RXIN_ESC2

2,3,4,5,6,7,8,9 A3V3 — A3V3
2,3,4,5,6,7,8,9 GND — GND

ESC2 Internal PHY RJ45 Connector - Port2 (DUT#3)



ESC2 Internal PHY RJ45 Connector - Port1 (DUT#2)



ASIX ELECTRONICS CORPORATION		
Title: P10-INT. PHY-DUT2/3		
Size: A3	Document Number: AX58101LT Junction Reference	Rev: 1.00
Date: Tuesday, August 26, 2025	Sheet 10 of 11	

Revision History

Revision	Date	Comment
V1.00	2025/06/23~ 2025/09/09	Initial release.

ASIX ELECTRONICS CORPORATION		
Title: P11-Revision History		
Size: B	Document Number: AX58101LT Junction Reference	Rev: 1.00
Date: Tuesday, September 09, 2025	Sheet 11 of 11	